REMARKS

The Office Action mailed May 4, 2005 has been carefully reviewed and the foregoing amendments and the following remarks are made in response thereto.

Claim 5 stands rejected under 35 U.S.C. § 112, ¶ 2, as being indefinite. Claims 1-6 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,841,663 to Sharma et al. (hereinafter "Sharma").

By this amendment, claim 5 has been amended to depend from dependent claim 4 which recites, *inter alia* "the entity portion of said description data is RTL description data." Thus, there is sufficient antecedent basis for the term "RTL description data in the entity portion" recited in claim 5. Applicant respectfully submits claim 5 now satisfies the requirements set forth by 35 U.S.C. § 112, ¶ 2. Withdrawal of the rejection is respectfully requested.

Claims 1 and 6 have been amended to further define the subject matter Applicant regards as the invention. Support for the amendments to claims 1 and 6 can at least be found in FIG. 2 of the present specification. Claims 2-4 remain unchanged in the application.

This amendment changes, adds, and/or deletes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier. Thus, claims 1-6 are presently pending in this application for consideration.

Applicant respectfully submits that each of the pending claims is patentably distinguishable over the cited reference as required by § 102. Applicant further submits that the cited reference fails to disclose the claimed method of generating an application specific integrated circuit (ASIC) design database. Independent claims 1 and 6 each have been amended to include steps of calculating and writing in the header, the simulation time, the layout area, the timing, and the power consumption data values. Sharma fails to disclose these claimed steps. This distinction will be further described below.

THE CLAIMS DISTINGUISH OVER THE CITED REFERENCE

Claims 1-6 stand rejected under 35 U.S.C. § 102(b) as being anticipated Sharma. Sharma is directed to a technique for synthesizing integrated circuits using a structured cell library with parameterized Hardware Description Library (HDL) modules. In Sharma, a datapath synthesizer accesses the library and assigns values to parameters to form specific implementations of the parameterized HDL modules. The specific implementations of the parameterized HDL modules are used by the datapath synthesizer to implement an HDL circuit description. Each parameterized HDL module includes an entity description, a behavioral description, and an implementation description (See, Abstract, lines 1-10).

The entity description specifies the parameters, input ports and output ports of a library circuit element. The behavioral description specifies the logical function performed by the library circuit element and the implementation description specifies how to construct the circuit element based on the parameter values (Column 1, line 65 – column 2, line 13). According to Sharma, having the datapath library of circuit elements described in an HDL allows one to specify a circuit element in a more general form and also allows the circuit elements to be simulated, verified and synthesized using widely available HDL simulation, verification and synthesis tools (Column 1, lines 45-51 and column 2, lines 30-32).

Unlike Sharma, Applicant's claimed invention is not directed to enhancing the description of the datapath library of circuit elements, but rather is directed to a method for generating an ASIC design database for reuse design and efficient information collection (Page 3, lines 8-13). A Register Transfer Level (RTL) description includes a header portion and an entity portion. According to one embodiment of the present invention, the header portion and the entity portion are unified and stored as one file in the database (Page 9, lines 1-3). As specifically recited by the steps of independent claims 1 and 6, four data values, the simulation time, the layout area, the timing, and the power consumption are calculated and then written in the header portion (See, Page 9, lines 11-15 and FIG. 3). For example, claim 1 now recites in pertinent part:

executing, when a function design using description data comprising a header portion and an entity portion has been performed, simulation by the simulation tool;

generating a simulation result list of the simulation;
extracting a simulation time from the simulation result list;
writing the extracted simulation time in the header portion of the description data;
inputting the entity portion of the description data to the logic synthesis tool and executing a logic synthesis;
outputting a gate-level net list;
inputting the net list to the timing analysis tool and executing a timing analysis;
outputting an analysis report as an analysis result;
comparing values in the analysis report with pre-input desirable specifications;
extracting, if the compared values satisfy the desirable specifications, timing information and layout area information, and writing the timing and layout area information in the header portion of the description data;
executing a logic simulation for the gate-level net list by the logic simulation tool;
inputting simulation data to the power consumption calculation tool and carrying out a power consumption calculation process;
outputting a power consumption calculation result list;
extracting power consumption information from the power consumption calculation result list and writing the power consumption information in the header portion of the description data; and
storing, as one file at a predetermined location, the description data comprising the header portion in which the information necessary for reuse is written, and the entity portion (Claim 1, lines 4-28).

Claim 6 recites similar steps.

Sharma does not disclose the steps of calculating and writing specific values in the header of the RTL description to create the ASIC design database. Instead, Sharma teaches using parameterized modules including the entity description, the behavioral description, and the implementation description stored in a library for designing circuits. As discussed above, there are no data values stored in the entity, behavior, or implementation description. Since Sharma does not disclose each of the steps claimed by Applicant, Sharma fails to anticipate independent claims 1 and 6. Thus, these claims are allowable.

Moreover, since independent claims 1 and 6 are allowable, claims 2-5 are also allowable by virtue of their direct or indirect dependence from allowable independent claim 1 and for containing other patentable features. Further remarks regarding the asserted relationship between any of the claims and the cited reference is not necessary in view of their allowability. Applicant's silence as to the Office Action's comments is not indicative of being in acquiescence to the stated grounds of rejection.

Accordingly, Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

Date September 6, 2005

By 41,179

FOLEY & LARDNER LLP
Customer Number: 22428
Telephone: (202) 945-6162
Facsimile: (202) 672-5399

Pavan K. Agarwal
Attorney for Applicant
Registration No. 40,888